

D/A0597
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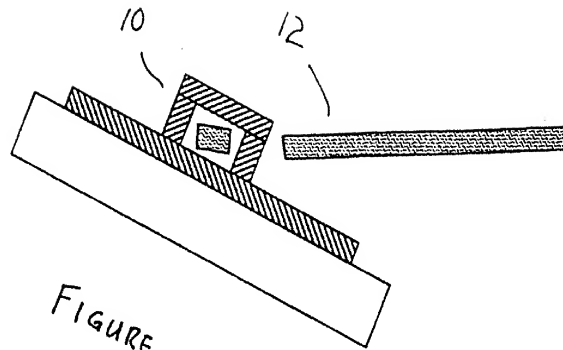


FIGURE 1

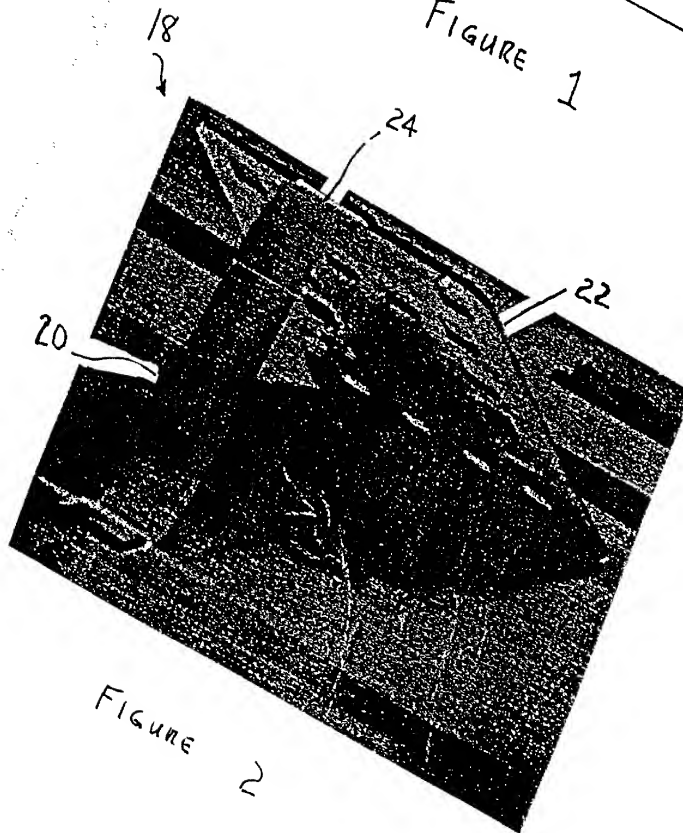


FIGURE 2

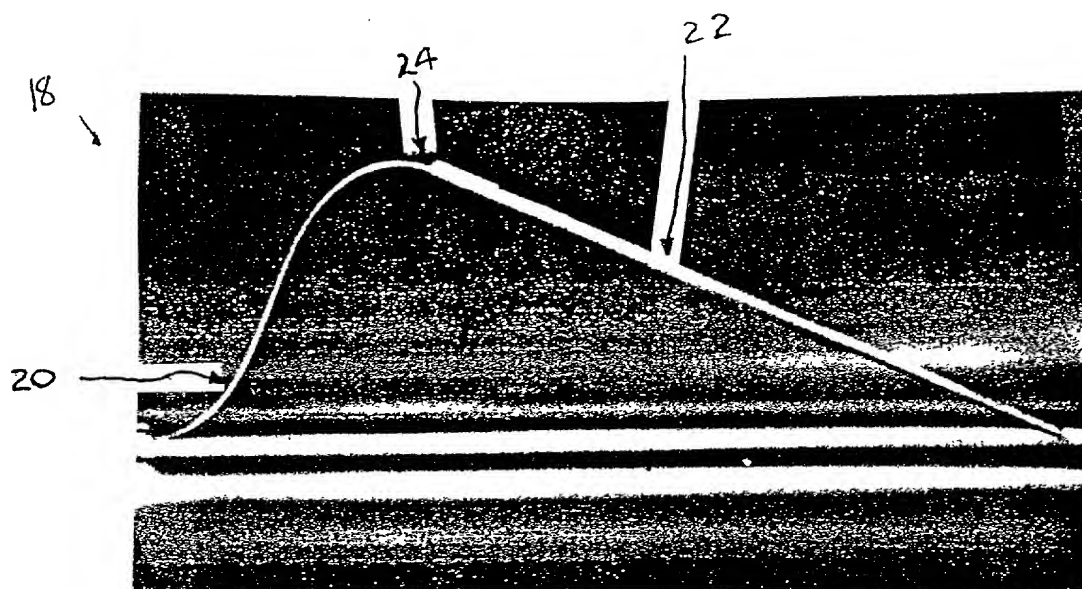
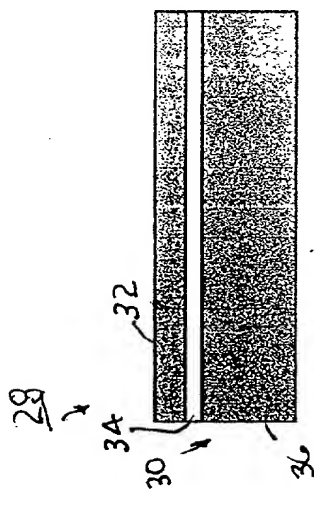
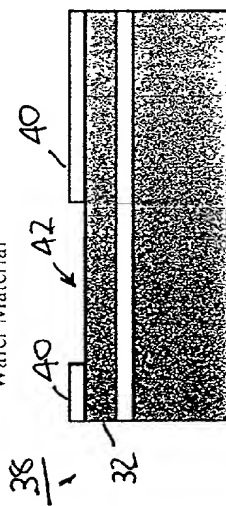


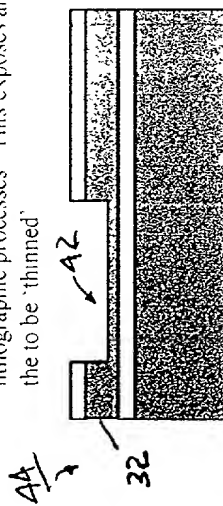
Figure 3



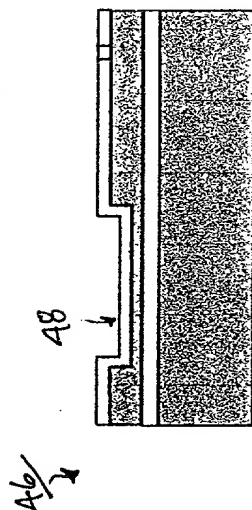
Start with cleaned SOI (Silicon On Insulator) Wafer Material



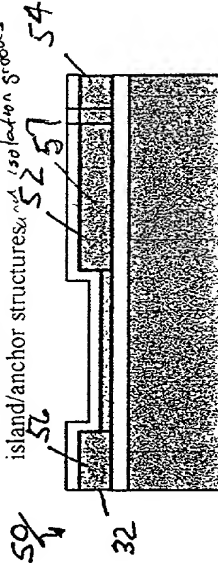
Deposit photoresist and pattern using std lithographic processes. This exposes area to be 'thinned'



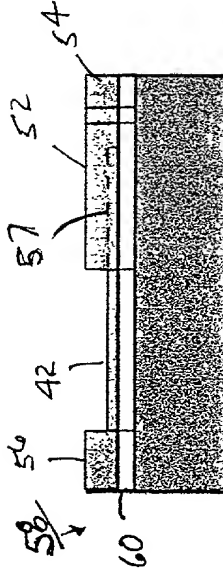
Wet etch (KOH 45% @ 60°C) exposed device layer silicon to a thickness of ~500nm



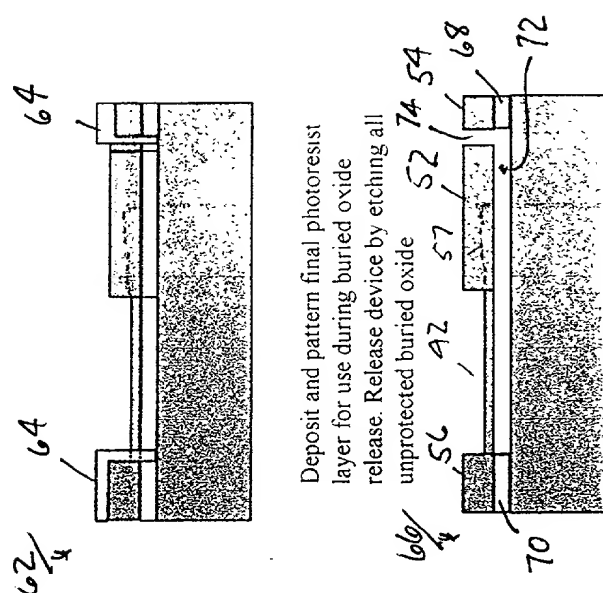
Remove previous resist layer before re-patterning for etch of mirror and island/anchor structures, and isolation grooves



Dry etch exposed silicon to form device structure



Remove photoresist and begin etching exposed buried oxide layer (using HF 49%)



Deposit and pattern final photoresist layer for use during buried oxide release. Release device by etching all unprotected buried oxide

Remove all remaining photoresist in dry O₂ plasma etch process

FIGURE 4

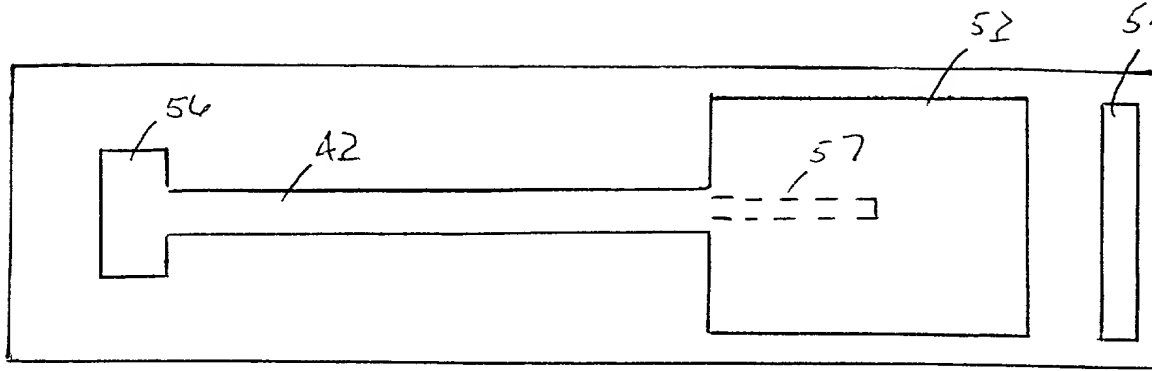


FIGURE 5

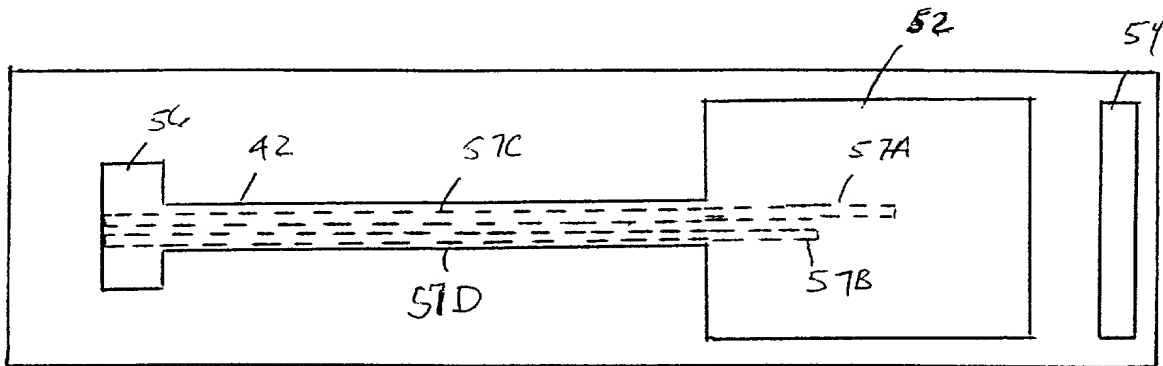


FIGURE 6

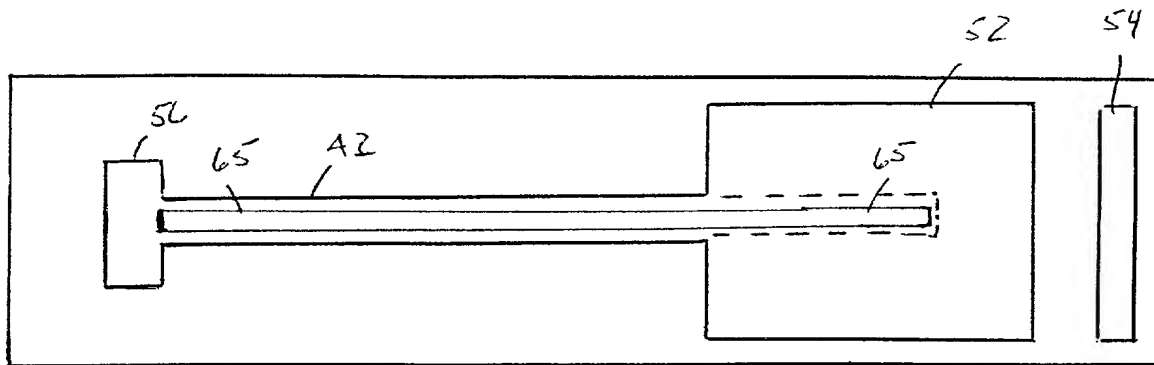


FIGURE 7

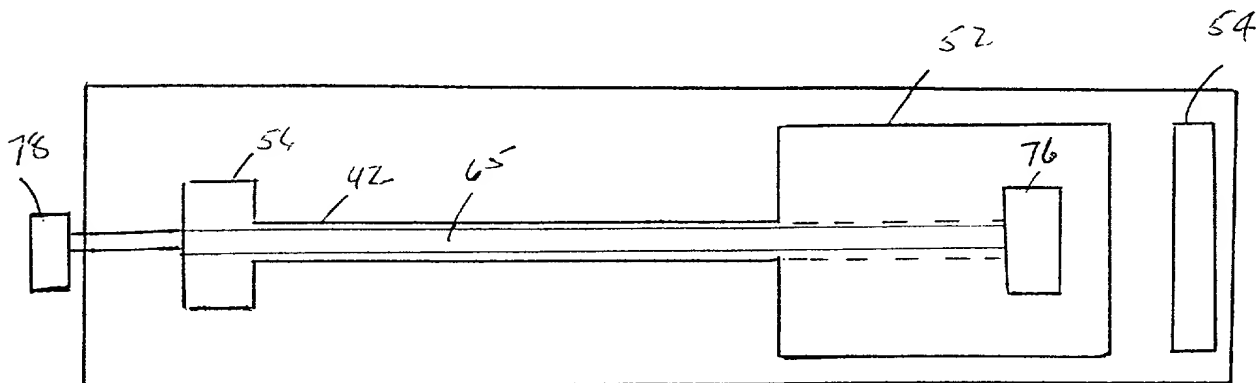


FIGURE 8